Dear Prof. Yaow-Ming Chen,

National Taiwan University, Taiwan

Editor-in-Chief,

IEEE Transactions on Power Electronics

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We would like to submit again the enclosed manuscript entitled “*Layout Based Ultra-Fast Short-Circuit Protection Technique for Parallel Connected GaN HEMTs,*” which we wish to be considered for publication in IEEE Transactions on Power Electronics. The paper is renovated and improved in the lights of previous supportive and helpful reviews. The novelty of the paper is sensing the induced voltage on the layout for detection of short-circuit fault on a parallel GaN HEMTs configuration. The implementation of short-circuit protection techniques on parallel configuration is not studied for GaN HEMTs in the literature. It is experimentally shown that the proposed method is able to detect short-circuit fault within 40 ns and it does not harm the normal switching operation.

We would like to highlight the improvements in this paper. For this purpose, the new content is highlighted and added at the end of submitted paper. Additionally, we addressed the helpful comments of the reviewers in the following pages.

The paper is composed according to IEEE Transactions on Power Electronics journal submission format. No conflict of interest exits in the submission of this manuscript, and manuscript is approved by all authors for publication. The paper is an original piece and not under consideration for publication elsewhere.

I appreciate your consideration of our manuscript, and I look forward to receiving comments from the reviewers.

Kind regards,

Dr. Ozan Keysan

**Reviewer 1 Comments**

**1)** *The Short-Circuit protection is very important for the safety of the converter operation. This paper presents a Short-Circuit protection technique by detecting the voltage on the power loop stray inductance of the test circuit. However, the detection scheme has been utilized in many previous studies:*

*[1] K. Sun, J. Wang, R. Burgos, and D. Boroyevich, “Design, analysis, and discussion of short circuit and overload gate-driver dual-protection scheme for 1.2 kV, 400 a SiC MOSFET modules,” IEEE Trans. Power Electron. vol. 35, no. 3, pp. 3054–3068, Mar. 2020.*

*[2] M. Oinonen, M. Laitinen, and J. Kyyr, “Current measurement and short-circuit protection of an IGBT based on module parasitics,” in Proc. 16th Eur. Conf. Power Electron. Appl., Aug. 2014.*

*[3] A. E. Awwad and S. Dieckerhoff, “Short-circuit evaluation and over-current protection for SiC power MOSFETs,” 2015 17th European Conference on Power Electronics and Applications, EPE-ECCE Europe 2015, 2015.*

Thank you for your comment. We have cited these papers in [8], [13], [14] in Section I. We indicated the differences of this study from the previous studies in seventh and eighth paragraph of Section I.

**2)** *This detection scheme is an effective way to detect Short-Circuit. Unfortunately, this paper does not provide any new idea to improve the detection scheme and is more like a case application. The innovation of this paper does not meet the standard of the TPEL.*

Thank you for your comment. We stressed better in Section V how important the outcome of this paper for application of short-circuit protection techniques on parallel switch configuration.

**3)** *Moreover, as far as I am concerned, this detection scheme may not be the best option for the GaN device. For the GaN device, due to its high switching speed, a large power loop stray inductance can induce false turn-on and self-sustained switching oscillation. To avoid this, the power loop stray inductance should be as small as possible. However, the detection scheme utilized intrusive to the circuit and generate additional stray inductance in the power loop. The detection scheme also requires the power loop stray inductance to be sufficiently large to generate a significant voltage drop for detection. This makes the test circuit even more vulnerable to the false turn-on and self-sustained switching oscillation.*

Thank you for your comment. We addressed the reviewer concern in the last paragraph of Section II-A, and in the last paragraph of Section III-A and we explained the advantages of the applied technique over other techniques in Section V.

**Reviewer 2 Comments**

1. *Why does “increased switching speed result in a dramatic increase in short circuit current under a shoot through fault”? The short circuit current in any case is limited by saturation of the device.*

Thank you for your comment. We have removed the given term in the abstract.

1. *In Fig 2, how are the components selected? Details must be shown.*

Thank you for your comment. We have explained component selection in Section III-A.

1. *The technique of using di/dt to trigger protection needs more justification. At the very least you must prove that the induced voltage in the sense loop under normal operation is lower than the induced voltage under shoot through fault. Showing one DPT test is not sufficient.*

Thank you for your comment. We have put much more waveform for Double Pulse Tests in Section IV. Figure 17, Figure 18 and Figure 19 and related comments highlight the differences of DPT and short-circuit fault.

1. *A good journal paper would characterize the induced voltage in the sense loop as a function of various parameters – loop sizes, trace thickness, load currents, voltages, gate resistances, etc. Since you have the FEA set up, you should be able to do this through simulations.*

Thank you for your comment. We have characterized the factors affecting induced voltage in equations (9) and (10) in Section II-A. We have explained the induction of voltage analytically in equations (12-16) in Section III-A.

1. *You need to justify why no blanking time is required. Usually we have blanking time to prevent switching-noise-related mis-triggering of the protection system. How do you distinguish between a normal switching event and a fault switching event?*

Thank you for your comment. The noise immunity and filter design are explained and verified by experiments in Sections III-B and IV. Figure 16,17 and 19 gives the experimental results for comparison of induced voltages for normal switching and short-circuit fault.

1. *The test protocol and the set of tests conducted are vastly under-reported. What type of short circuit tests are these? Fault under load (FUL)? Hard switching fault (HSF)? It would be helpful to see a simple diagram showing the timing of different events during your tests – Fig 9 is not easy to understand.*

Thank you for your comment. The fault type is given 8th paragraph of Section I. The test protocol is given in second paragraph of Section II-A and timing diagram of short-circuit protection is changed in a more understandable way as shown in Figure 14 and it is discussed in third paragraph of Section IV in detail.

1. *The test results shown in Fig 9 are also insufficient to conclude successful detection and interruption of the short circuit current. In particular, the device current and voltage waveforms need to be shown. How can we be sure this was done at 400V dc? What peak current did the device reach? Was this test repeated multiple times? Results like Fig 9 also need a more detailed narration to explain each of the traces.*

Thank you for your comment. Measurement of short-circuit current is explained in second paragraph of Section IV. The voltage waveform is shown in Fig. 14 in Section IV. The test is repeated for different operating points and results are given in Fig. 16. Fig. 9 is replaced with Fig. 14 and it is explained in third paragraph of Section IV in detail.

1. *The need for soft turn off is already shown in previous papers. While Fig 10 reconfirms this point, what new information is it adding?*

Thank you for your comment. The importance of the corresponding figure (Fig. 15) is explained in the third paragraph of Section IV.

1. *The double pulse test shown in Fig 11 does not prove too much. Many problems occur after the device has heated up and is operating in a noisy environment.*

Thank you for your comment. The filter design is explained in detail in Section III-B. Moreover, this design is verified by experiments where the results are given in Section IV. Figure 16, 17, 18 and 19 compares the regular switching and short-circuit faults cases. The effect of temperature unfortunately could not be measured due to insufficient facility.

1. *Table II makes the point that this is the only work using parallel devices. But why does this matter? Do the other methods not work for parallel devices, or did they just not show it? What were the unique challenges with short circuit protection of parallel devices (vs single devices)?*

Thank you for your comment. We have discussed the implementation of different methods given in Table II on parallel configuration in Section V. Figure 20 visualizes how to utilize different methods for parallel devices. The unique challenges and the performance comparison of all methods are given in third, fourth, fifth, sixth paragraphs of Section V.

**Reviewer 3 Comments**

1. *In Fig. 9, could you show Vds?*

Thank you for your comment. Fig. 9 is replaced with Fig. 14 including drain-source voltage waveform.

1. *In Fig.3, Vgs is +6/-3V. However, according to Fig.9 and Fig.11, it can be found that Vgs is +6/-4V in the practical application.*

Thank you for your comment. Fig. 3 is replaced with Fig.4 with the correction of negative gate drive level as -4V.

1. *[14] also used the parasitic inductance for current detection. Therefore, Comparing with [14], please further explain the contribution or the advantage of this paper.*

Thank you for your comment. The unique challenges of short-circuit protection for parallel configuration is discussed in detail in Section V. The Section VI is modified to show novelty in this paper as well.

1. *In this paper, a portion of the return path is the inductance for current detection, which is the part of the layout parasitics parameters. Therefore, this paper seems to work on reducing the parasitics inductance which is used to realize the short-circuit protection, instead of proposing the new short-circuit protection method.*

Thank you for your comment. The effect of power loop inductance is expressed in first paragraph of Section II. The dynamics of sensing the fault is explained in Section II-A. Moreover, layout design considerations are given in Section III-A. Lastly, the differences in layout design for parallel and single bridge configurations are given in third, fourth and fifth paragraphs of Section V.

1. *The short-circuit protection is triggered by sensing the voltage across the layout inductance. However, high di/dt at normal operations may cause false-triggers. The highest di/dt that the protection circuit can withstand should be provided to verify the noise immunity of the protection circuit. Besides, the di/dt of GaN HEMTs during normal operations should be discussed in this paper.*

Thank you for your comment. In order to highlight the noise immunity of protection circuit Section III-B is added. Filter design is verified by experimental results and given in Section IV. Fig.19 verifies the filter design by comparing FFT plots for regular switching and short-circuit fault cases.

1. *In Fig.11, the dv/dt of GS66508T under 400V, 25A is provided, in which the turn-on dv/dt is only 16.9V/ns and the turn-off dv/dt is only 39.9V/ns. However, in “Analysis of the dv/dt Transient of Enhancement-Mode GaN FETs”, GS66508P is tested. The result shows that the turn-off dv/dt of GS66508P under 20A is about 100V/ns, and the turn-on dv/dt is about 150-200 V/ns at any current. From the datasheet, it can be found that GS66508P is very close to GS66508T. why the dv/dt in your paper is much lower than that shown in other papers?*

Thank you for your comment. We have investigated the paper given above. The given dV/dt values in that paper are the peak values during the switching transient. We have shown the average transition speed in Fig. 17. We have indicated this difference in fifth paragraph of Section IV.

**Reviewer 4 Comments**

1. *The short circuit protection method has already been published in [14], except for the additional feature that more FETs can be paralleled in this work.*

Thank you for your comment. The novelty of this paper expressed better in Section V in detail.

1. *Discussions on the circuit operating principle, finite-element simulations, characterization results are mostly qualitative that lack more in-depth quantitative analysis and insights, which would make it more difficult for readers to appreciate this work.*

Thank you for your comment. We have characterized the factors affecting short-circuit dynamics in equations (1-10) in Section II-A. The induced voltage is analytically expressed in equations (12-16) in Section III-A. The filter design is formulated in equations (17-18) in Section III-B.

1. *Why a negative voltage of -4 V is used for off-state Vgs of a normally-off power transistor (See the waveform in Fig. 9)?*

Thank you for your comment. The necessity of negative gate drive voltage level is explained in second paragraph of Section II-A.

1. *In Table I, how is each time interval determined?*

Thank you for your comment. The question of the reviewer is addressed in second paragraph of Section IV.

1. *No particular focus has been placed on the study and analysis of the technique implemented for multiple FETs in parallel, even if it should have been one of the highlights of this manuscript.*

Thank you for your comment. We improved the paper to highlight the unique challenges of parallel connection. Prior studies focusing on short-circuit fault of parallel devices are cited in seventh paragraph of Section I. Moreover, we have discussed the implementation of different methods given in Table II on parallel configuration in Section V. Figure 20 visualizes how to utilize different methods for parallel devices. The unique challenges and the performance comparison of all methods are given in third, fourth, fifth, sixth paragraphs of Section V. The Section VI is modified to show novelty in this paper as well.