Dear Prof. Yaow-Ming Chen,

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Editor-in-Chief,

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We would like to submit again the enclosed manuscript entitled “*Layout Based Ultra-Fast Short-Circuit Protection Technique for Parallel Connected GaN HEMTs,*” which we wish to be considered for publication in IEEE Transactions on Power Electronics. The paper is renovated and improved in the lights of previous supportive and helpful reviews. The novelty of the paper is sensing the induced voltage on the layout for detection of short-circuit fault on a parallel GaN HEMTs configuration. It is experimentally shown that the proposed method is able to detect short-circuit fault within 40 ns and it does not harm the normal switching operation.

We would like to highlight the changes we made since reviews given before:

In the light of supportive comments of first reviewer, we stressed better in Section V how important the outcome of this paper for application of short-circuit protection techniques on parallel switch configuration. We addressed the reviewer concern, “*The detection scheme utilized intrusive to the circuit and generate additional stray inductance in the power loop.*”, in Section II-A and in Section III-A and we explained the advantages of the applied technique over other techniques in Section V.

In the light of supportive comments of second reviewer, we explained how the components are selected in Section III-C. We characterized the parameters affecting induced voltage under a short-circuit fault analytically and showed in Section II-A. The noise immunity and filter design are explained and verified by experiments in Sections III-B and IV. The test protocol and fault type are given in Section II-A and timing diagram of short-circuit protection is changed in a more understandable way as shown in Figure 14 and it is discussed in Section IV in detail. The performance of short-circuit protection method is shown experimentally for different operating points and given in Figure 16. The valuable comment of the reviewer “*The need for soft turn off is already shown in previous papers. While Fig 10 reconfirms this point, what new information is it adding?*” is addressed in Figure 15. To the knowledge of authors, the importance of soft turn-off is known by the engineers in general inherently but it is now shown experimentally in the papers related to short-circuit protection in the literature. The double pulse test results are expanded to show sensed voltage for regular switching in Figure 17. The sensed voltage is shown for different bias voltages and loadings in Figure 18. Finally, FFT comparison is given in Figure 19 for regular switching and short-circuit fault to verify filter design given in Section III-B. The valuable comment of the reviewer “*Table II makes the point that this is the only work using parallel devices. But why does this matter? Do the other methods not work for parallel devices, or did they just not show it? What were the unique challenges with short circuit protection of parallel devices (vs single devices)?”* helped us to explain better the importance of the techniqueand the advantages of the proposed short-circuit protection method and the unique challenges of short-circuit protection with parallel devices are discussed in Section V.

In the light of supportive comments of third reviewer, we show the drain-source voltage waveform under short-circuit fault in Figure 14. The gate driving voltage levels are changed so that experimental results match with the Figure 4. The improvements in this paper over the paper, which was published before by the authors for single-bridge configuration, is explained better in Section V. The valuable comment of the reviewer, “*This paper seems to work on reducing the parasitics inductance which is used to realize the short-circuit protection, instead of proposing the new short-circuit protection method.”*, is addressed through the paper. Minimizing power loop inductance is clearly a must for the sake of healthy switching. The layout based short circuit protection methods are mostly criticized for increasing the power loop inductance. Therefore, we think it is important to stress that the proposed method does not deteriorate the power loop inductance. Moreover, the layout design is much harder for parallel devices and need to be explained to address the concerns of the reader. The noise immunity and filter design are explained and verified by the experiments in Sections III-B and IV. The FFT comparison is given in Figure 19 for regular switching and short-circuit fault to verify filter design given in Section III-B. The valuable comment of the reviewer, “*In Fig.11, the dv/dt of GS66508T under 400V, 25A is provided, in which the turn-on dv/dt is only 16.9V/ns and the turn-off dv/dt is only 39.9V/ns. However, in “Analysis of the dv/dt Transient of Enhancement-Mode GaN FETs”, GS66508P is tested. The result shows that the turn-off dv/dt of GS66508P under 20A is about 100V/ns, and the turn-on dv/dt is about 150-200 V/ns at any current. From the datasheet, it can be found that GS66508P is very close to GS66508T. why the dv/dt in your paper is much lower than that shown in other papers?”*, is analyzed by the authors. The paper shared by the reviewer investigates the dV/dt transient of GaN FETs and the givcn dV/dt values by the reviewer are the peak dV/dt values during the switching transient. These values are different from our values given in Figure 17 since we show the average dV/dt values during the switching transient.

In the light of supportive comments of forth reviewer, the improvements in this paper over the paper, which was published before by authors for single-bridge configuration, is explained better in Section V. Paralleling devices changes the difficulty level of implementation of short-circuit protection methods as discussed in Section V. A better analytical approach is given in Section II-A to characterize the factors affecting short-circuit fault. The valuable comment of the reviewer, *“Why a negative voltage of -4 V is used for off-state Vgs of a normally-off power transistor (See the waveform in Fig. 9)?”,* is addressed in Section IV. The non-monolithic GaN HEMTs, which are driven by an external gate driver circuit which increases the gate loop inductance, are subject to false turn-on risk as explained in [5]. Due to the gate loop inductance, the gate voltage of transistor increases during the switching as shown in Figure 17. Therefore, a negative gate bias is applied to keep this level below threshold. The valuable comment of the reviewer, “*In Table I, how is each time interval determined?*”, is addressed in Figure 14 and Table I. We measured the time intervals using the experimental waveforms on oscilloscope (LeCroy WaveRunner 44-Xi, 5GSa/s). We discussed the importance of the proposed method for parallel FETs in Section V. The techniques reported in the literature are visualized in Figure 20, to explain the weak and strong points of each method in a better way for parallel configuration.

The paper is composed according to IEEE Transactions on Power Electronics journal submission format. No conflict of interest exits in the submission of this manuscript, and manuscript is approved by all authors for publication. The paper is an original piece and not under consideration for publication elsewhere.

I appreciate your consideration of our manuscript, and I look forward to receiving comments from the reviewers.

Kind regards,

Dr. Ozan Keysan